

SOLAR-CELL INTERCONNECT DESIGN FOR TERRESTRIAL PHOTOVOLTAIC MODULES

G. R. Mon, D. M. Moore, and R. G. Ross, Jr.

Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
Pasadena, California 91109

ABSTRACT

An investigation of interconnect fatigue in photovoltaic systems has led to the development of useful reliability-design and life-prediction algorithms presented here. Experimental data gathered in this study indicate that the classical strain-cycle (fatigue) curve for the interconnect material is a good model of mean interconnect fatigue performance, but fails to account for the broad statistical scatter, which is critical to reliability prediction. To fill this shortcoming the classical fatigue curve is combined with experimental cumulative interconnect failure-rate data to yield statistical fatigue curves (with failure probability as a parameter) that enable (1) the prediction of cumulative interconnect failures during the design life of an array field, and (2) the unambiguous--i.e., quantitative--interpretation of data from field-service qualification (accelerated thermal-cycling) tests.

Optimal interconnect cost-reliability design algorithms are derived, intended to minimize the cost of energy over the design life of the array field. This procedure yields not only the minimum break-even cost of delivered energy, but also the required degree of interconnect redundancy and an estimate of array power degradation during the design life of the array field. The usefulness of the design algorithms is demonstrated with realistic examples of design optimization, prediction, and service qualification testing.

INTRODUCTION

Comprehensive investigations of failure modes affecting photovoltaic module performance and reliability are a major effort of the Engineering Sciences Area of the Jet Propulsion Laboratory's Flat-Plate Solar Array Project. The objective of this research is to define means of reducing the cost and improving the utility and reliability of photovoltaic modules for the broad spectrum of terrestrial applications. It is in this light that this paper addresses the interconnect failure problem.

Interconnect failure is induced by diurnal thermal cycles, which cause the distance between adjacent cells to expand and contract, thereby straining the interconnect(s) joining them. After a number of such cycles, depending upon the strain levels induced in each interconnect, microcracks develop and eventually propagate across the width of the interconnect until separation (open circuit) occurs. Thus the underlying failure mechanism is mechanical fatigue.

Metallurgists characterize fatigue by means of empirical strain-cycle (fatigue) curves that define the mean number of cycles to failure vs the strain level in the subject material. However, the life of any individual interconnect is governed by its flaw strength as determined by such agents as metallurgical defects and

manufacturing variations in shaping and attachment. The result is that each interconnect fails randomly, yet the fraction of equally strained interconnects that fail in an arbitrarily chosen time interval is statistically predictable.

When every interconnect connecting an adjacent cell pair has failed, the substrating containing that cell pair can no longer deliver its energy to the load; the result of interconnect failures is thus degradation of array power output. The use of redundancy in the deployment of interconnects can decrease the rate of degradation and, in fact, a sufficiently high degree of redundancy can reduce the degradation to negligible levels. Excessive interconnect redundancy, however, is costly. Economic considerations dictate a tradeoff between the degree of redundancy (cost) and the rate of power reduction (performance). This tradeoff is achieved by minimizing the cost of energy generated over the life of the array.

Module-interconnect reliability design and life-prediction procedures are presented herein that enable the module manufacturer to:

- (1) calculate interconnect strain levels for a particular module-interconnect design configuration;
- (2) predict the cumulative interconnect failure fraction at end-of-array-life, assuming interconnect fatigue to be the only active failure mechanism;
- (3) estimate array power degradation;
- (4) determine the degree of interconnect redundancy necessary to achieve minimum life-cycle cost of energy over the intended life of the array; and
- (5) establish the maximum allowable fraction of interconnect failures, and hence a non-arbitrary pass-fail threshold, in an accelerated thermal-cycling test.

MODULE INTERCONNECT DESIGN PROCEDURE

Interconnect analysis and design for photovoltaic arrays, particularly for space applications, are well documented (1). It is known that good interconnect design practice requires:

- (1) minimizing the thickness;
- (2) maximizing the expansion loop height;
- (3) maximizing the length, i.e., the distance between interconnect-to-cell attachment points; and

- (4) Avoiding solder and/or adhesive overflow onto the interconnect, which effectively shortens its active length, thereby overstraining the interconnect material.

Each of these techniques reduces the effective strain range (i.e., the maximum peak-to-peak strain in the interconnect material, hereinafter called the strain), thereby prolonging interconnect life.

An effective process of module-interconnect design involves comparing the predicted end-of-design-life cumulative interconnect failure probability, calculated for a definite module-interconnect design and site-specific temperature and insolation history, with a table of maximum allowable interconnect failure probabilities determined from considerations of end-of-life array power reduction and circuit and interconnect redundancy, for which minimum life-cycle energy costs have been determined. In addition to minimum cost, this comparison yields the required interconnect redundancy and provides an estimate of the end-of-life array power reduction. The design procedure is presented in Fig. 1.

In the following three sections the analytical procedures represented by the rectangles in Fig. 1 will be presented, with examples, in summary form. The reader desiring detailed exposition is referred to a report (2) that treats this subject comprehensively.

INTERCONNECT FAILURE PREDICTION

This section outlines a procedure for computing cumulative interconnect failure probability at end-of-life starting with a specific module-interconnect design concept and deployment site temperature history. Steps include computing interconnect displacement, computing interconnect material strain, and computing interconnect failure probability.

Computing Interconnect Displacement

The first step is to determine the effective thermally induced change δ in the distance g between points where

the interconnect is attached to adjacent cells (Fig. 2). This effective thermal displacement δ is determined from module design, geometry, and material properties, and site-dependent average diurnal temperature variations.

The total diurnal temperature change may be taken as

$$\Delta T = \Delta T_D + \Delta T_{Op} \quad (1)$$

where

ΔT_D = difference between daily high and low ambient temperatures

ΔT_{Op} = module operating temperature above ambient (about 30°C for most module designs at 100 mW/cm² irradiation)

The effective interconnect displacement is given by

$$\delta = [(\alpha_s - \alpha_c)C + (\alpha_c - \alpha_I)g]\Delta T \quad (2)$$

where

δ = effective change in the distance between attachment points

C = center-to-center distance between cells

D = solar cell diameter

g = distance between attachment points of the interconnects

α_s = thermal expansion coefficient of the substrate or superstrate

α_c = thermal expansion coefficient of the solar cells

α_I = thermal expansion coefficient of the interconnect material

ΔT = diurnal temperature variation

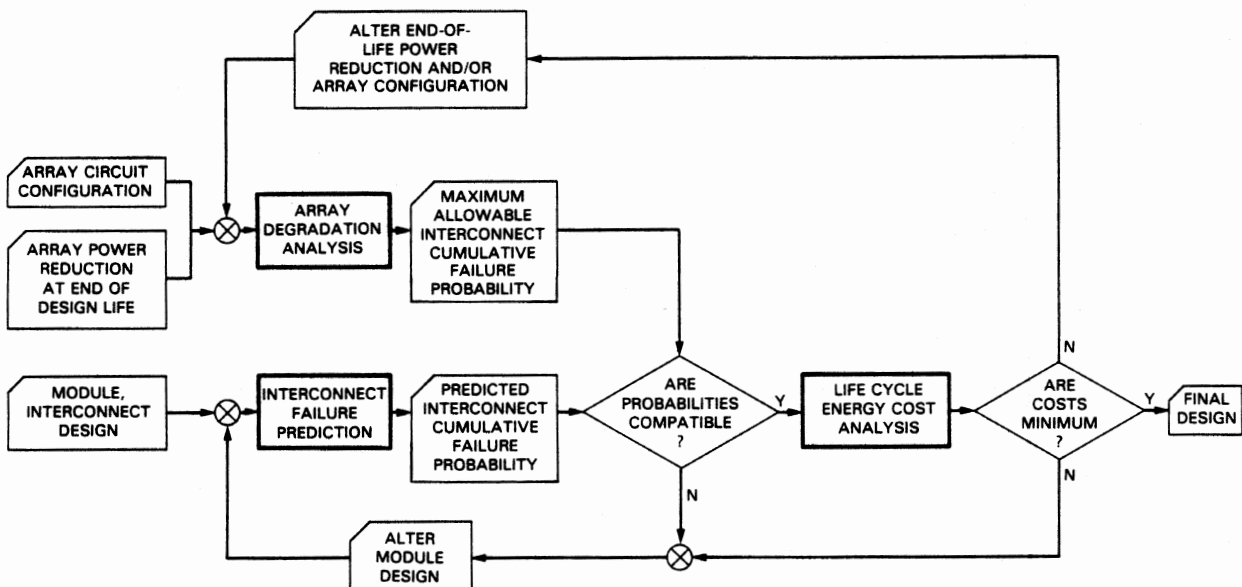


Fig. 1. Module Interconnect Design Procedure

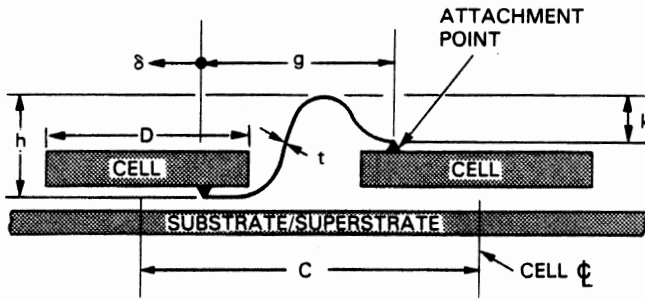
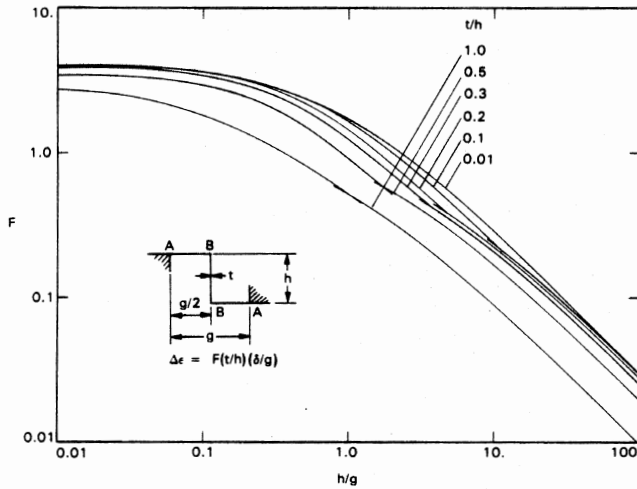


Fig. 2. Module Interconnect Geometry

Computing Interconnect Material Strain

Having determined the interconnect displacement δ from temperature variations, the next step is to calculate the total strain range $\Delta\epsilon$ induced in the interconnect material by the displacement δ . For complex interconnect configurations this step requires computer assistance using finite element modeling techniques of structural analysis. To circumvent the time and cost inherent in computer use, nomographs have been developed in this study to permit rapid graphical determination of strain levels in several important interconnect configurations (2). A representative nomograph is presented in Fig. 3.



- Notes: 1. g is the Horizontal Distance Between Interconnect Attachment Points.
2. Maximum Strain Above Break in Curves Occurs Between Points B, Below Break in Curves Between Points A and B.

Fig. 3. Shape Factor F for Z-Type Interconnect

The maximum strain in the interconnect can be expressed as

$$\Delta\epsilon = F \cdot \left(\frac{t}{h}\right) \cdot \left(\frac{\delta}{g}\right) \quad (3)$$

where

$\Delta\epsilon$ = maximum strain in the interconnect

t = thickness of interconnect

h = height of interconnect

δ = effective change in attachment-point-to-attachment-point dimension

g = attachment-point-to-attachment-point dimension

F = shape factor computed using the nomograph, Fig. 3

Computing Interconnect Failure Probability

Having determined maximum interconnect strain from displacement δ , the final step is to calculate the predicted fraction p_f of interconnects (the interconnect failure probability) that will fail in a specified number of cycles. This is achieved through the use of statistical fatigue curves, a set of standard strain-cycle curves parameterized by the interconnect cumulative failure probability. Statistical fatigue curves have been generated by combining experimental cumulative interconnect failure-rate data with the interconnect-material empirical fatigue curve.

Empirical Fatigue Curve

The interconnect material fatigue curve provides the basis for computing interconnect life. This curve is given by an empirical formula suggested by Manson (3) who demonstrated its universality in describing the fatigue behavior of 29 different metals and alloys:

$$\Delta\epsilon = 3.5 \frac{\sigma_u}{E} N^{-0.12} + \ln\left(\frac{1}{1-RA}\right) 0.6 N^{-0.6} \quad (4)$$

where

$\Delta\epsilon$ = total interconnect strain range (elastic plus plastic)

σ_u = ultimate tensile strength of material

E = Young's modulus

RA = reduction in area (from tensile test)

N = number of cycles to failure

For OFHC 1/4-hard copper, the interconnect material studied in this investigation, property values used are

$$\sigma_u = 0.262 \text{ GPa}$$

$$E = 117.2 \text{ GPa}$$

$$RA = 0.70$$

giving

$$\Delta\epsilon = 0.0078 N^{-0.12} + 1.1178 N^{-0.60} \quad (5)$$

This curve is plotted in (A) of Fig. 4.

Various experimental data are also plotted in Fig. 4. Several modules of diverse design were thermal-cycle tested to as much as 575 cycles. At the end of the test, broken interconnects were counted, their shapes were measured, and the strains in them were calculated using the nomographs (2).

These data are plotted in (B) of Fig. 4 as a cloud of points between $N = 47$ cycles and $N = 575$ cycles. Their distribution about the fatigue curve is evidence supporting the argument that the empirical fatigue curve adequately represents interconnect fatigue behavior.

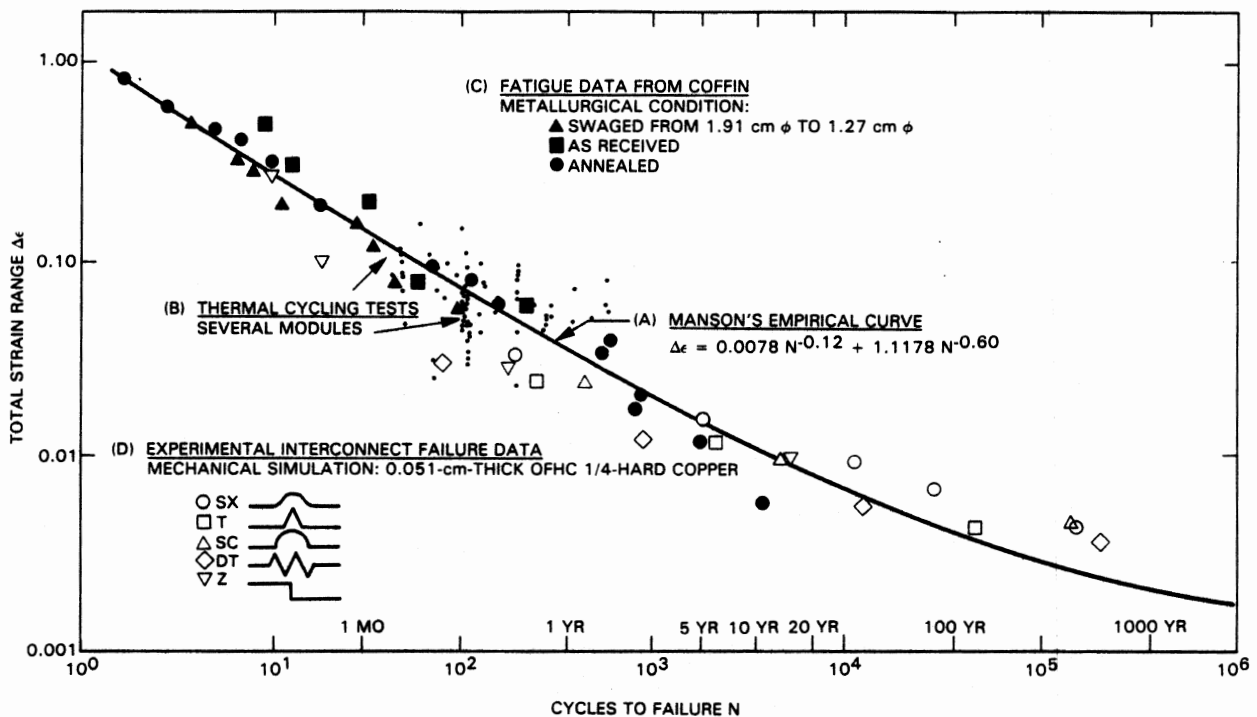


Fig. 4. Fatigue Information: OFHC Copper

The shaded points (C) in Fig. 4 represent conventional mechanical fatigue data for OFHC copper in widely varying metallurgical conditions (4). Manson's curve also agrees well with these data.

To achieve further understanding of interconnect fatigue statistics, a large number of interconnects were fabricated and tested to failure in this study. Test specimens are 0.051-mm-thick OFHC 1/4-hard copper interconnects shaped by precisely machined dies to the configuration shown in Fig. 5. In each test 30 specimens of the same configuration are carefully mounted on the test fixture shown in Fig. 6. This device consists of two horizontal plates vertically offset 0.254 mm to simulate the thickness of a typical solar cell and horizontally separated by a nominal 1.905-mm gap to simulate a typical cell-to-cell gap in a module. One plate is then made to move horizontally back and forth relative to the other at a constant (but adjustable) cycle rate and amplitude. The interconnects are series-wired so that, when a break occurs, the cycling ceases. The number of cycles to failure of each interconnect is recorded and testing continues until the next failure or the end of the test.

The raw data obtained from this testing procedure are presented in Fig. 7 as a plot of cumulative interconnect-failure probability vs the number of cycles to failure. The data curves are labeled with the number of interconnects of the particular configuration tested and with the strain range $\Delta\epsilon$ calculated using a finite-element program or the nomographs developed in this study (2). Each unshaded data point (D) in Fig. 4 is obtained from a single one of the test curves in Fig. 7, giving a plot of strain range $\Delta\epsilon$ vs the number of cycles at which the cumulative interconnect failure probability is 0.50. Manson's curve can thus be regarded as a 50% failure-probability curve. For periods of present interest to module designers (5 to 30 years), the curve underestimates experimentally observed interconnect

longevity; this conservatism makes the curve useful as a predictive and design tool.

Statistical Fatigue Curves

Manson's empirical fatigue curve relates interconnect strain level to the number of cycles at which the cumulative interconnect failure fraction is 0.50. For interconnect and array field life prediction, it is of greater value to have a set of curves relating strain level to cycles-to-failure for a wide range of cumulative interconnect failure fractions. Such a set of curves can be obtained by combining failure rate data from the mechanical simulation tests with the empirical fatigue curve.

This is achieved by first superposing all of the data curves of Fig. 7 at the $p_I = 0.50$ point, Fig. 8, and observing that all curves have approximately the same slope (failure rate) in the region of high cumulative failure probability, $0.2 \leq p_I \leq 1.0$, and that the curves for some interconnect configurations exhibit long tails in the region of low cumulative failure probability, $0.0 \leq p_I \leq 0.2$. Then fitting the failure data from each region to a two-parameter Weibull cumulative failure distribution function yields

$$\frac{N_p}{N_{0.50}} = 2.621 \left(\ln \frac{1}{1-p_I} \right)^{1.214}, \quad 0 < p_I < 0.2 \quad (6)$$

and

$$\frac{N_p}{N_{0.50}} = 1.224 \left(\ln \frac{1}{1-p_I} \right)^{0.537}, \quad 0.2 < p_I < 1.0 \quad (7)$$

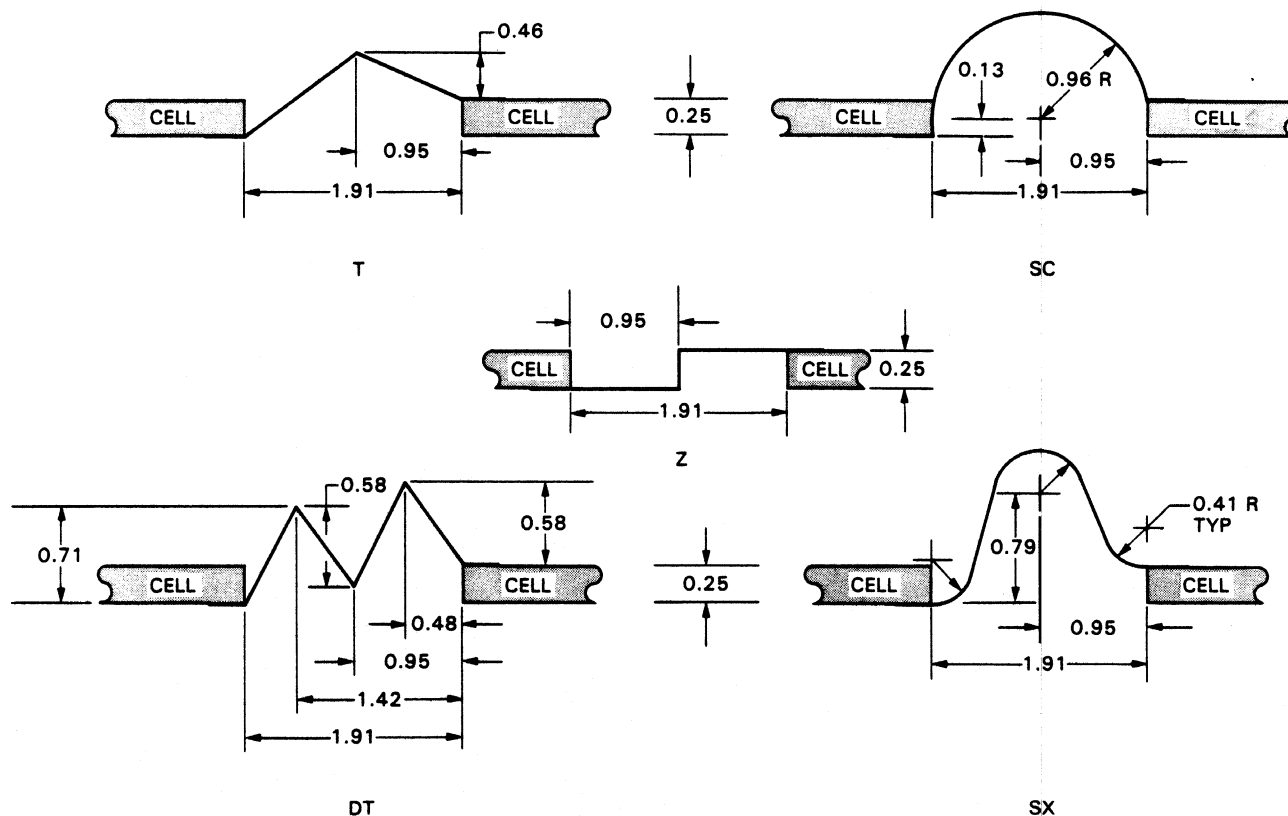


Fig. 5. Geometry of Interconnects Mechanically Cycled to Failure and Their Code Designations (all dimensions are in millimeters)

In these equations

P_I = cumulative interconnect failure probability

N_p = number of cycles to achieve a cumulative failure probability p

$N_{0.50}$ = number of cycles to achieve a cumulative failure probability of 0.50.

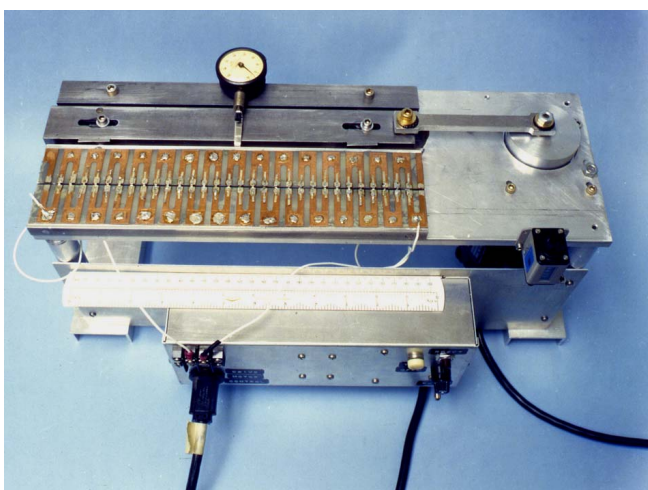


Fig. 6. Interconnect Strain-Cycle (Fatigue) Apparatus

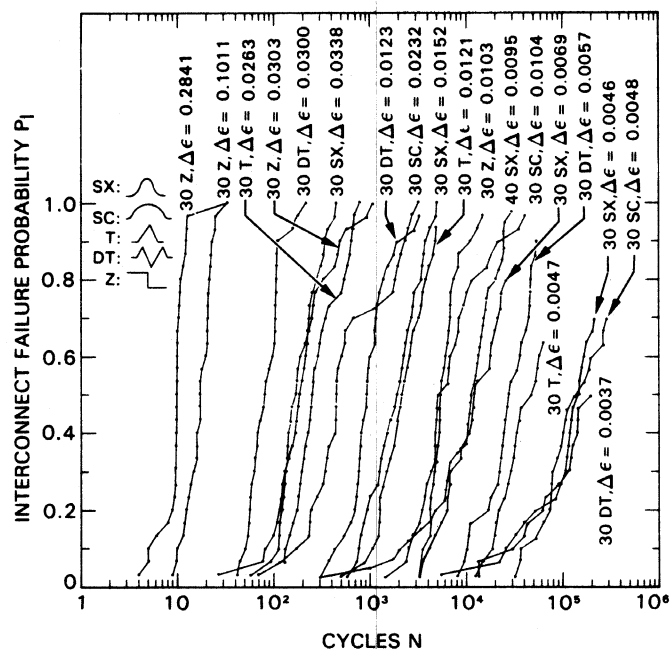


Fig. 7. Experimental Failure Probability vs Number of Cycles to Failure for 0.051-mm-Thick OFHC Interconnect Configurations

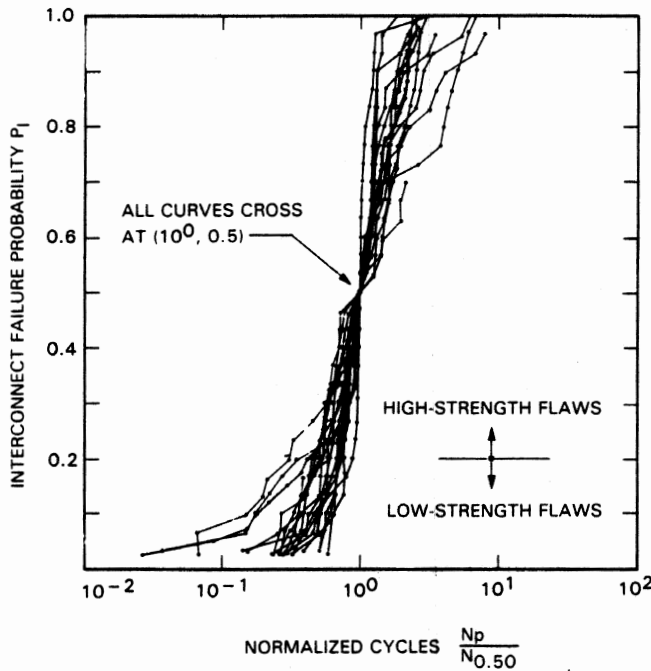


Fig. 8. Superposition of Test Data Curves for Failure-Rate Determination

Substituting these equations into the Manson formula, Equation (5) gives, for $0 \leq P_I \leq 0.20$,

$$\Delta\epsilon = 0.0088 \left[N_p \ln \left(\frac{1}{1 - P_I} \right) \right]^{-1.214}^{-0.12} + 1.9929 \left[N_p \left(\ln \frac{1}{1 - P_I} \right) \right]^{-1.214}^{-0.60} \quad (8)$$

and, for $0.20 < P_I < 1.0$,

$$\Delta\epsilon = 0.0080 \left[N_p \left(\ln \frac{1}{1 - P_I} \right) \right]^{-0.537}^{-0.12} + 1.2616 \left[N_p \left(\ln \frac{1}{1 - P_I} \right) \right]^{-0.537}^{-0.60} \quad (9)$$

These last equations are used to generate the statistical fatigue curves of Fig. 9 and 10, which relate the variables strain range, life, and failure probability. It is assumed that early interconnect failures can be attributed to low-strength flaws, and later failures to high-strength flaws; this provides the rationale for the designation of the two failure ranges in Fig. 8.

Fig. 10 can now be used to complete the interconnect failure prediction calculation. Having previously computed the interconnect strain range $\Delta\epsilon$, one enters the graph in Fig. 10 with this strain value as ordinate. The appropriate end-of-life curve is then used to determine the abscissal value P_I of interconnect failure probability.

An Example

Consider as an example a module-interconnect design representative of present module construction, viz., a

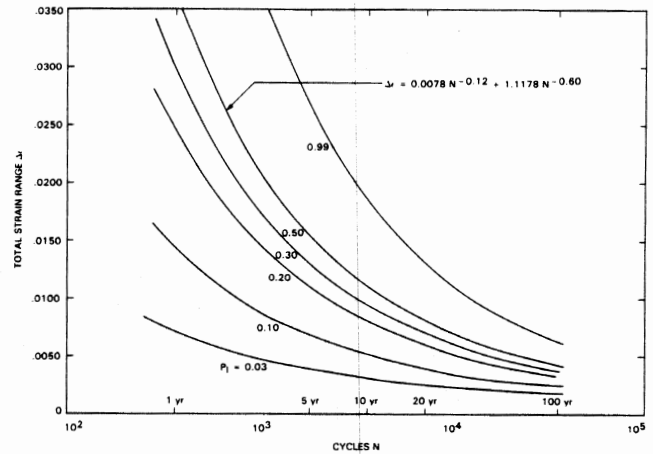


Fig. 9. Statistical Fatigue Curve for OFHC Copper Interconnects With Failure Probability as Parameter

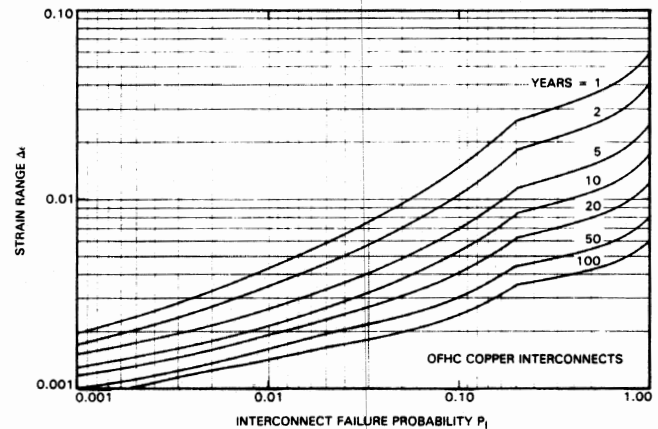


Fig. 10. Interconnect Strain Range $\Delta\epsilon$ vs Interconnect Failure Probability P_I with Array Life (years) as Parameter

glass-superstrate module with Z-type interconnects. The design parameters are: $\alpha_g = 9.2 \times 10^{-6}$ cm/cm/°C (glass), $\alpha_c = 2.9 \times 10^{-6}$ cm/cm/°C (silicon), $\alpha_I = 5.3 \times 10^{-6}$ cm/cm/°C (copper), $C = 10.16$ cm, $D = 9.96$ cm, $g = 6.35$ mm, $t = 0.051$ mm, and $h = 0.305$ mm. Equation (2) with $\Delta T = 46^\circ\text{C}$, typical of many sites across the country, gives $\delta = 0.0029$ cm and the Z-type interconnect nomograph gives $F = 4.0$. It follows from Equation (3) that $\Delta\epsilon = 0.0031$. The life prediction curves, Fig. 10, predict a cumulative interconnect failure probability of $P_I = 0.054$ in 20 years (5.4% interconnect failures in 20 years).

ARRAY DEGRADATION ANALYSIS

The module interconnect design procedure presented in Fig. 1 enables the designer of photovoltaic modules to determine the degree of interconnect redundancy required to achieve minimum cost and acceptable end-of-design-life array power reductions. The interconnect failure prediction algorithm presented in the previous section, provides a means of predicting the fraction of failed interconnects at end-of-life for a particular module interconnect design.

In this section a companion algorithm is presented that generates the interconnect failure fraction p_I associated with a specified end-of-life array power-loss fraction f_y and degree of interconnect redundancy r . The designer can compare his predicted failure fractions with a table of failure probabilities generated from considerations of array power degradation to determine the degree of interconnect redundancy that will result in acceptable array power reductions.

The dependence of array power degradation on circuit redundancy (series-parallelism) has been illuminated by Ross (5). Fig. 11 illustrates this dependency for a limited range of array series-parallel-diode configurations. A voluminous parametric analysis (6,7) has yielded many such curves, which (with additional array circuit design considerations) are collected in (8).

The substring and interconnect failure probabilities are numerically related as follows:

$$p_c = p_I^r \quad (10)$$

and

$$F_{ss} = 1 - (1 - p_c)^n \quad (11)$$

where

F_{ss} = substring failure probability

n = number of parallel interconnect groups per substring (see Fig. 12)

p_c = cell failure probability

r = degree of interconnect redundancy

p_I = interconnect failure probability

The array power-loss fraction is assumed to result from substring failures caused by interconnect failures only.

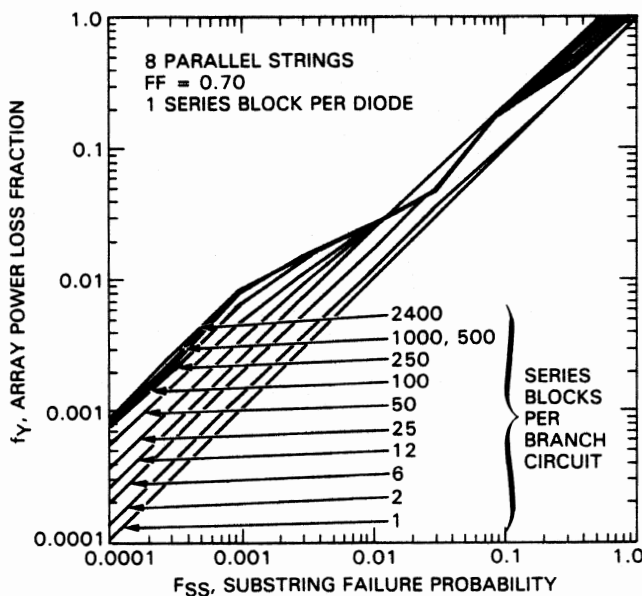


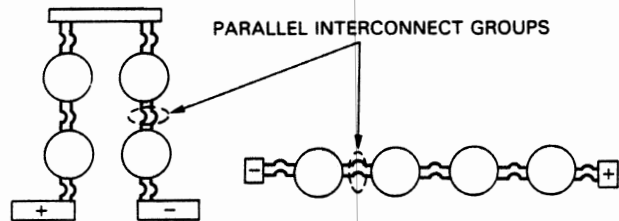
Fig. 11. Array Power Loss

$$F_{ss} = 1 - (1 - p_c)^n$$

F_{ss} = SUBSTRING FAILURE PROBABILITY

p_c = CELL FAILURE PROBABILITY

n = NUMBER OF PARALLEL INTERCONNECT GROUPS PER SUBSTRING



EXAMPLE: 4 CELLS,
 $r = 2$
 $n = 6$

EXAMPLE: 4 CELLS,
 $r = 2$
 $n = 5$

Fig. 12. Relation Between Substring and Cell Failure Probabilities

An Example

To demonstrate the use of the array degradation algorithm, consider the example array design presented in Table 1.

Table 1. Example Design Parameters

Array configuration:

- (1) OFHC copper interconnects.
- (2) 8 parallel by 11 series cells per series block:
 $n = 12$.
- (3) 57 series blocks per branch circuit.
- (4) 1 series block per diode.
- (5) $V_{array} = 250$ V.

Design objectives:

- (1) 20-year array power reduction.
- (2) Interconnect failure probability.
- (3) Minimum life-cycle energy cost.
- (4) Required interconnect redundancy.

The array degradation will be determined for a 20-year cumulative interconnect failure fraction $p_I = 0.054$ and an interconnect redundancy $r = 3$. Using these figures in Equation (10) gives a cumulative cell failure probability $p_c = 1.58 \times 10^{-4}$. Then Equation (11) with $n = 12$ (see Fig. 12) gives a substring failure probability $F_{ss} = 0.00189$. Entering Fig. 11 with this value as abscissa and using the curve corresponding to 57 series blocks per branch circuit (interpolation required), it is determined that the array power loss fraction at 20 years is $f_y = 0.0088$ (power down 0.88%).

In this fashion an entire table (Table 2) of power reductions associated with specific failure probabilities and interconnect redundancies has been generated. The strain values listed in Table 2 were determined from the probabilities using the 20-year curve of Fig. 10.

Table 2. Array Power Reduction at 20 years

20-Year PI	Maximum Allowable Strain $\Delta\epsilon$	Array Power Reduction at 20 years f_y					
		$r = 1$	2	3	4	5	6
0.005	0.0016	0.125	0.0018	0	0	0	0
0.010	0.0019	0.240	0.0059	0	0	0	0
0.050	0.0031	0.71	0.05	0.0070	0.0004	0	0
0.100	0.0040	0.96	0.24	0.029	0.0055	0.0007	0
0.150	0.0049	1.00	0.31	0.054	0.019	0.005	0.0013
0.200	0.0062	1.00	0.57	0.19	0.038	0.013	0.003
0.300	0.0069	1.00	0.90	0.46	0.20	0.048	0.023
0.400	0.0075	1.00	1.00	0.90	0.45	0.26	0.085
0.500	0.0081	1.00	1.00	1.00	0.80	0.53	0.32

Table 2 suggests two generalizations:

- (1) Adding interconnects, i.e., increasing redundancy, dramatically reduces the array power loss rate over the 20-year array life.
- (2) Allowing a higher maximum strain results in considerably larger power loss rates.

These observations are not surprising, but the large sensitivity of array power loss to variations in strain is.

LIFE-CYCLE ENERGY COST ANALYSIS

As was indicated in the previous section, the end result of interconnect failures is degradation of array power output. It was also shown that design techniques such as redundant interconnects can decrease the rate of degradation to negligible levels. Excessive interconnect redundancy, however, is costly. Economic considerations dictate a tradeoff between the degree of redundancy (cost) and the rate of power reduction (performance). This tradeoff is described in this section; it is achieved by minimizing the cost of energy generated over the life of the array.

The cost of energy over the lifetime of the array field is determined by equating the worth of delivered energy to the cost of obtaining that energy. Letting R represent the (constant) cost of energy, it follows (2, 5, 9) that

$$R = \frac{C_B + \frac{C_A + C_I + C_M}{\eta}}{I_0 \epsilon_{LC}} \quad (12)$$

where

R = constant worth of energy over array lifetime, \$/kWh

C_B = balance of plant costs, \$/kW

C_A = initial array costs less redundant interconnects, \$/m²

C_I = estimated add-on cost of interconnects per square meter of module area, \$/m²

C_M = life-cycle operation and maintenance costs, \$/m²

η = plant efficiency (100 mW/cm², NOCT)

I_0 = annual solar insolation, kWh/m²/year

ϵ_{LC} = life-cycle energy fraction

The life-cycle energy fraction ϵ_{LC} is the present value of energy output over the life of the array; for zero discount rate, it is determined as the area under the curve of power output fraction $1 - f_y$ vs array operation time (2).

Equation (12) provides the basis for conducting the economic tradeoff between interconnect fatigue life, interconnect redundancy, array degradation, and the fabrication costs associated with the various interconnect options.

An Example

To illustrate application of Equation (12) consider again the example design problem defined in Table 1. The assumed system cost and performance parameters that are independent of the interconnect design are presented in Table 3. Assumed add-on costs for just the interconnects are presented in Table 4 as a function of interconnect redundancy. The objective of the analysis is to determine the appropriate choice of interconnect redundancy in light of the costs, array degradations, and interconnect failure probabilities.

Table 3. Design Example Cost Parameters

Balance of plant costs	$C_B = 250$ \$/kW
Initial array costs less redundant interconnects	$C_A = 113$ \$/m ²
Operation and maintenance costs	$C_M = 0$
Total plant efficiency	$\eta = 0.092$
Annual insolation	$I_0 = 2000$ kWh/m ² /yr

Table 4. Add-On Costs for Interconnects

Interconnect Redundancy r	Estimated Costs for Interconnects C_I , \$/m ² of Module Surface
2	4.22
3	5.05
4	6.18
5	7.75
6	9.99

The results of the analysis (2), are displayed in Table 5. It is evident from Table 5 that life-cycle costs increase with increasing failure probability. Minimum costs for a given maximum allowable failure probability are boxed. It is noted that cost optimization requires that modules be designed for operation at low strain levels, although the variation in costs over the two-orders-of-magnitude range of interconnect failure probabilities is small. It is also noted that the various cost minima are relatively flat; e.g., at $p_I = 0.05$, the cost difference in using three, four, or five interconnects is negligible. This is surprising, considering

Table 5. Life-Cycle Energy Costs

20-Year p_I	Maximum Allowable Strain $\Delta\epsilon$	Life-Cycle Energy Cost \$, \$/kWh					
		$r = 1$	2	3	4	5	6
0.005	0.00160	0.0415	0.0382	0.0383	0.0386	0.0391	0.0397
0.010	0.00188	0.0445	0.0383	0.0384	0.0386	0.0391	0.0397
0.050	0.00305	0.0632	0.0392	0.0385	0.0387	0.0391	0.0397
0.100	0.00404	0.0960	0.0419	0.0388	0.0387	0.0391	0.0397
0.150	0.00487	0.1680	0.0462	0.0392	0.0389	0.0391	0.0397
0.200	0.00624	0.3285	0.0577	0.0415	0.0395	0.0393	0.0397
0.300	0.00693	0.4284	0.0680	0.0448	0.0414	0.0397	0.0399
0.400	0.00752	0.4620	0.0770	0.0505	0.0452	0.0418	0.0414
0.500	0.00808	0.4928	0.0856	0.0581	0.0495	0.0449	0.0443

the extremely large variation in array power reduction for these degrees of redundancy (Table 2).

For the example module following the Static Fatigue Curves section, for which $p_I = 0.054$, the degree of interconnect redundancy and associated 20-year array power reduction can now be determined for the example array field under consideration. Table 5 suggests three interconnects per parallel interconnect group, giving a minimum cost of delivered energy of 0.0385 \$/kWh. The array power loss fraction at 20 years (Table 2) is an acceptable 0.0088 (see example following Equation 11).

THERMAL CYCLING TESTING

Thermal cycling testing of modules is performed to qualify modules for field application. One test profile in common use is shown in Fig. 13; the most recent test specifications require $N = 200$ test cycles (10). For this test profile, $\Delta T_{\text{test}} = 130^\circ\text{C}$. Then for a site for which $\Delta T_{\text{field}} = 46^\circ\text{C}$,

$$\Delta\epsilon_{\text{test}} = \frac{\Delta T_{\text{test}}}{\Delta T_{\text{field}}} \Delta\epsilon_{\text{field}} = 2.83\Delta\epsilon_{\text{field}} \quad (13)$$

In order to determine the maximum allowable number of interconnect failures in the test, use is made of the statistical fatigue curve, Fig. 9, reproduced in Figure 14. An example in the figure shows that qualification for 20-year service at a 10% cumulative interconnect field-failure level requires that there be less than 4.2% failures at 200 test cycles. This type of calculation is continued to generate Fig. 15, which gives the maximum allowable interconnect test failure level for a specified number of test cycles to qualify a module for 20-year service at a typical field site for which $\Delta T \approx 46^\circ\text{C}$. The example on the graph indicates that the test failures should not exceed 4.2% at 200 cycles to qualify

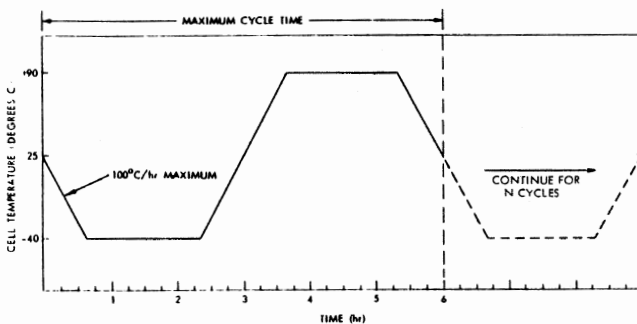
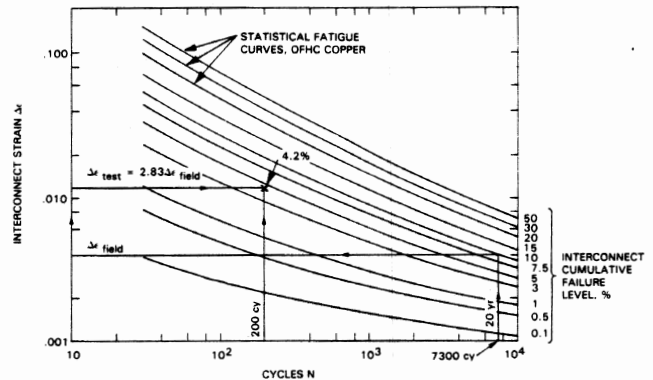
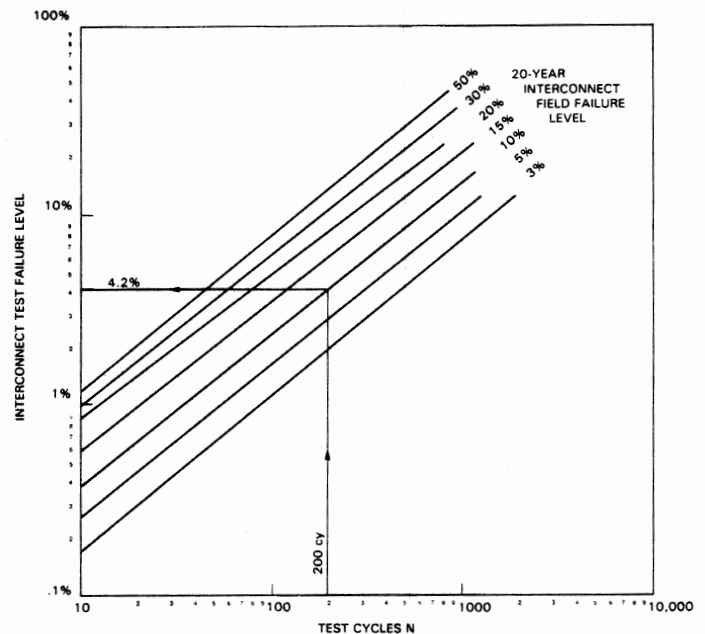


Fig. 13. Thermal-Cycling Test Conditions

Fig. 14. Thermal Cycle Test Design for Module Qualification at Typical Site ($\Delta T \approx 46^\circ\text{C}$)Fig. 15. Maximum Allowable Interconnect Test Failure Level for a Specified Number of Test Cycles with Field Failure Level as Parameter (Qualification for 20-Year Service at $\Delta T \approx 46^\circ\text{C}$)

a module for 20-year service at a 10% field-failure level.

Table 6 presents thermal cycling test data and results from several differently designed modules. Pass-fail judgments are based on the criteria established in Fig. 15. The field-failure level for which the module is being qualified is seen to be an important factor in making pass-fail judgments.

Finally, because the purpose of thermal cycling testing is to provide type approval of a particular module design, a number of modules from the same lot--enough to provide at least 300 interconnects--should be tested in order to present a believable statistical picture of interconnect failures for that design.

Table 6. Module Qualification: 20-Year Service
at $\Delta T \approx 46^\circ\text{C}$

Thermal Cycle Test Results

Type of Module	No. Thermal Cycles $\Delta T = 130^\circ\text{C}$	Observed Test Failure Level, %	Qualification for 10% Field Failure Level		Qualification for 5% Field Failure Level	
			Max. Allowable Test Failure Level, %	Judgment	Max. Allowable Test Failure Level, %	Judgment
Randomly Oriented	297	67	5.9	Failed	3.8	Failed
Glass Fiber Substrate	575	69	9.8	Failed	6.3	Failed
	297	36	5.9	Failed	3.8	Failed
	575	69	9.8	Failed	6.3	Failed
	297	31	5.9	Failed	3.8	Failed
Superstrate	247	0	5.0	Passed	3.2	Passed
Superstrate	446	3	8.0	Passed	5.2	Passed
Superstrate	397	0	7.3	Passed	4.7	Passed
Substrate	547	6	9.3	Passed	6.2	Marginal
	547	10	9.3	Failed	0.2	Failed
Substrate	497	0	8.7	Passed	5.6	Passed
	497	7	8.7	Passed	5.6	Failed

DISCUSSION

Discussion of the test and design philosophy, and suggested directions for future research, follow:

- (1) This investigation focused upon the thermally induced mechanical-fatigue failure of interconnects. The design and cost-optimization algorithms are predicated on the assumption that array power loss is attributable solely to interconnect failures, to the exclusion of such other contributing effects as cell breakage, encapsulation discoloration, electrical insulation failure, etc. A logical extension of this work is the incorporation of these and other factors into the design and cost algorithms.
- (2) Although the fatigue curves presented in this paper are limited to copper interconnects, the procedures developed are general. Another phase of this research involves the study of aluminum and clad metals. Aluminum exhibits fatigue behavior similar to that of copper and is much less expensive. Clad metal interconnects, on the other hand, although more expensive to manufacture, exhibit none of the fabrication problems associated with aluminum interconnects and in addition may offer improved resistance to fatigue failures.
- (3) Elastic behavior on the part of the interconnect has been assumed in this study in using the finite-element modeling procedure to calculate interconnect strains. In reality, however, interconnect behavior is largely plastic. Two factors justify using elastic analysis to determine strain in interconnects behaving plastically in service. The first is cost; the cost of performing plastic analysis is prohibitive. The second is that elastic analysis yields good results (it works) as is evident from the data of Fig. 4. In that figure, the plotted experimental data points for which strain levels have been computed agree well with the empirical elastic-plastic fatigue curve of the interconnect material.
- (4) The large temperature range of the module thermal cycling test and the rapid cycling of

interconnects in the mechanical simulation tests--both contrary to existing field conditions--may be questioned. Most investigators seem to disregard cycle rate and moderate temperature extremes as influential factors in the mechanical fatigue of metals. The various experimental data presented in Fig. 4 agree well with one another despite considerable variation in cycle rate. The mechanical simulation tests are conducted at 30 cycles per minute, the thermal cycling test at 4 cycles per day. The data of Coffin and Tavernelli (4) were obtained at 7 to 16 cycles per minute, and field cycles are 1 per day.

The fundamental requirement of an accelerated test is that it not introduce degradation modes not active in the intended application. Enhanced temperature range (thermal-cycling tests) or lack thereof (mechanical simulation test) were not observed to violate this requirement. In fact, many degradation modes are suppressed in such tests, e.g., hail impact, wind loading, etc., but these modes do not generally contribute substantially to interconnect failures. The major interconnect failure mechanism is thermally induced strain cycling (3), i.e., fatigue, and the primary cause of premature interconnect failure is faulty module-interconnect design.

CONCLUDING REMARKS

Interconnect fatigue performance has been characterized by the interconnect material fatigue curve. Nomographs have been developed to facilitate the computation of interconnect strain. Based on the interconnect material fatigue curve and experimental failure rate data, array life prediction has been demonstrated. A design algorithm has been developed enabling the selection of minimum-cost redundant interconnect systems. Thermal cycling testing of modules for the purpose of characterizing interconnect performance has been given a quantitative foundation--particularly in regard to acceptance-or-rejection threshold levels.

ACKNOWLEDGMENTS

This paper presents the results of one phase of research conducted at the Jet Propulsion Laboratory, California Institute of Technology, for the U.S. Department of Energy, by agreement with the National Aeronautics and Space Administration.

We extend our deepest gratitude to our technician Betty Jetter, who conducted the mechanical simulation testing with noteworthy skill, concern, and enthusiasm.

We also extend thanks to Solarex Corp., which provided the interconnect material for the mechanical simulation tests described in this paper.

REFERENCES

1. Solar Cell Array Design Handbook, JPL Report SP-43-38, Vol. I and II, October 1976.
2. Mon, G.R., Moore, D.M., and Ross, R. G., Jr., Interconnect Fatigue Design for Terrestrial Photovoltaic Modules, JPL Document 5101-173, Jet Propulsion Laboratory, Pasadena, California, in press.
3. Manson, S.S., "Fatigue: A Complex Subject--Some Simple Approximations," Experimental Mechanics, pp. 193-226, July 1965.

4. Coffin, L.F., Jr., and Tavernelli, J.F., "The Cyclic Straining and Fatigue of Metals," Transactions of the Metallurgical Society of America, Vol. 215, pp. 794-807, October 1959.
5. Ross, R.G., Jr., "Flat-Plate Photovoltaic Array Design Optimization," Proceedings of the 14th IEEE Photovoltaic Specialists Conference, pp. 1126-1132, 1980.
6. Gonzalez, C.C., and Weaver, R., "Circuit Design Considerations for Photovoltaic Modules and Systems," Proceedings of the 14th IEEE Photovoltaic Specialists Conference, pp. 528-535, 1980.
7. Weaver, R., "Flat-Plate Photovoltaic Array Simulation and Design Analysis," Proceedings of the Systems Simulation and Economic Analysis Conference, SERI/TP - 351-431, pp. 105-112, January 1980.
8. Flat-Plate Photovoltaic Module and Array Circuit Design Optimization Workshop Proceedings, JPL Internal Document 5101-170, Jet Propulsion Laboratory, Pasadena, California, May 1980.
9. Ross, R.G., Jr., "Photovoltaic Design Optimization for Terrestrial Applications," Proceedings of the 13th IEEE Photovoltaic Specialists Conference, pp. 1067-1073, June 1978.
10. Block IV Solar Cell Module Design and Test Specification for Intermediate Load Center Applications, JPL Document 5101-16, Revision A, Jet Propulsion Laboratory, Pasadena, California, November 1978.